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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/849,707	05/04/2001	Gregory J. Smith	50019.57USU1/P04868	9655

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EXAMINER	
NGUYEN, DANNY	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 06/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/849,707	SMITH ET AL.	
	Examiner	Art Unit	
	Danny Nguyen	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,12-15 and 17-19* is/are rejected.

7)☒ Claim(s) *8-11,16 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 12 and 17 are objected to because of the following informalities: pages 19 and 20, lines the phase " the shunt circuit is activated during the normal operation..." should be "the shunt circuit is deactivated during the normal operation. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Fortune (USPN 5,333,105).

Regarding to claim 1, Fortune discloses a protection circuit (18 shown in fig. 1) that is arranged to coupled to a fast transient signal (20) to a control terminal (the output from the shunt controller 32) in response to a fast transient event such that the shunt circuit (38) is activated in response to the fast transient signal and the shunt circuit is protected from the fast transient event.

Regarding to claim 3, Fortune discloses the protection circuit (18) comprises a resistance circuit (resistor coupled between the output from the shunt controller (32) and the gate of the transistor 90 shown in fig. 2) is arranged such that a voltage drops

across the resistance circuit in response to the transient and the voltage drop activates the shunt circuit (90) such that the shunt circuit is protected from the transient (col. 2, lines 41-65).

Regarding to claim 4, Fortune discloses the shunt circuit (38) comprises a field effect transistor (90) couples power from the power supply terminal (via lead 40) and a ground terminal (via lead 42) in response to a control voltage that associated with the control terminal (the output from the comparator 32). Wherein the control circuit couple to the fast transient signal to the gate of shunt transistor (90) in response the transient event such that the transistor (90) is activated an a fast voltage transient associated with the power supply terminal (20) is discharged to the ground.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2, 5-7, 12-15, 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fortune in view of Ker et al. (USPN 6,249,410).

Regarding to claims 2, 5, 6, Fortune discloses all limitations of claim 1 except for having a capacitance circuit. Ker et al. disclose a capacitor (50 shown in fig. 4). It would have been obvious to one having skill in the art to modify the circuit of Fortune with a

capacitor as taught by Ker et al. in order to bypass an ESD current and dissipate the electrostatic charge from the source (Ker et al. col. 3, lines 19-22).

Regarding to claim 7, Fortune discloses the resistance circuit (the resistor connects to the output from the amplifier (32) to the control gate of the shunt transistor (90)) to provide the control signal to the control terminal. Fortune does not disclose a capacitor coupled between the control terminal and the power line. Ker et al. disclose a capacitor (50) coupled between the control terminal (the gate of transistor 10) to the power line (input pad 5) (shown in fig. 4). It would have been obvious to one having skill in the art to modify the circuit of Fortune with a capacitor as taught by Ker et al. in order to bypass an ESD current and dissipate the electrostatic charge from the source (Ker et al. col. 3, lines 19-22).

Regarding to claims 12, 14, 15,17, Fortune discloses an error amplifier (32) that is arranged to produce a control signal (the output form the circuit 32) at a control terminal in response to a reference voltage (coupled to the circuit 32 via lead 30) and a voltage at a power supply terminal (20), a resistance circuit (the resistor connected between the gate of the shunt transistor 90 with the conductor 22) produces another control signal in response the fast transient, a shunt circuit (38) coupled from the power supply terminal (20 via lead 40) the ground terminal when activated, wherein the shunt circuit is deactivated by the control signal during normal operation and the shunt circuit is activated by the another control signal by the control signal during the fast transient such that the excess energy is shunted from the power terminal (20) to the ground by providing the another control signal to the control terminal in a time interval that is

shorter than the amplifier response time (col. 4, lines 20- 33). Fortune does not disclose a capacitance circuit as claimed. Ker et al. disclose a capacitor (50) coupled the input terminal (5) to the control gate of the transistor (see fig. 4). It would have been obvious to one having skill in the art to modify the circuit of Fortune with a capacitor as taught by Ker et al. in order to bypass an ESD current and dissipate the electrostatic charge from the source (Ker et al. col. 3, lines 19-22).

Regarding to claim 13, Fortune discloses the shunt circuit (38) includes a transistor (90) coupled power from the power supply (20) and the ground (22).

Regarding to claims 18, 19, Fortune discloses a method of protecting a shunt circuit regulator (fig. 2) comprises the steps of detecting the fast transient (by shunt controller 32, col. 2, lines 41-47), providing a current in response to the fast transient (the output from the controller 32 in term of current, col. 4, lines 21-23), producing the voltage in response to the current, coupling the voltage to a control terminal of the shunt device (the gate of the transistor 90) such that the voltage activates the shunt device (col. 2, lines 45-61), and coupling power from the power supply (20) through the shunt device (38 via lead 40) to the ground (via lead 42), when the shunt device is active, the shunt device protected from the fast transient. Fortune does not disclose a capacitance circuit as claimed. Ker et al. disclose a capacitor (50) coupled the input terminal (5) to the control gate of the transistor (see fig. 4). It would have been obvious to one having skill in the art to modify the circuit of Fortune with a capacitor as taught by Ker et al. in order to bypass an ESD current and dissipate the electrostatic charge from the source (Ker et al. col. 3, lines 19-22).

Allowable Subject Matter

4. Claims 8, 9, 10, 11, 16, 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claim 8 recites the shunt circuit comprises a plurality of transistors that are arranged to couple power from a power supply terminal to a circuit ground in response to a control voltage that is associated with the control terminal, wherein the protection circuit is arranged to couple to the fast transient signal to each gate of the plurality of the transistors in response to the fast transient such that each of the plurality of the transistors is activated and the transient discharged to the ground.

Claims 16, 20, recites an apparatus and method of protecting the shunt circuit comprises steps of detecting a slow ESD event with a master ESD protection circuit, producing an ESD detection signal in response to the slow ESD event, activating at least one slave ESD protection circuit, and providing a discharge path from the supply terminal to the ground through the at least the slave ESD protection circuit.

The references of record do not teach or suggest the aforementioned limitation, nor would it be obvious to modify those references to include such limitation.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is (703)-305-5988. The examiner can normally be reached on Mon to Fri 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703)-308-3119. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-872-9318 for regular communications and (703)-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-0956.

DN

DN
May 30, 2003

GREGORY J. TOATLEY, JR.
PRIMARY EXAMINER